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Characteristics of a symmetrical Cockcroft-Walton power supply of 50 Hz 1.2 MV/50 mA

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A 1.2 MV/50 mA symmetrical Cockcroft-Walton (SCW) power supply of over 83% power efficiency, driven by 50 Hz frequency, was developed for an industrial electron beam irradiator. It is constructed by capacitors of 45 nF and 28.13 nF in the coupling column and capacitors of 18.75 nF in the smoothing column. Working status of the rectifier in high power output condition was analyzed, and the conduction angle of the rectifier was calculated. The power factor (*PF*) of the SCW circuit has been studied, and the equivalent condensance of the circuit has been derived. Measurements were done for the *PF* compensation. The surge impact during the short circuit transient process was considered in choosing the protection resistance. Test results showed that design specifications of the power supply were achieved, with the non-load voltage being up to 1.32 MV and the ratio of ripple voltage to output voltage as 9.4%. © *2011 American Institute of Physics*. [doi:10.1063/1.3592597]

I. INTRODUCTION

Since Cockcroft and Walton adopted the cascade circuit in their proton accelerator,[1] various kinds of improved circuit were developed to power the CW-type accelerators. Henneberke adopted 500 Hz converter as the power of a 7-stage CW generator with 1.5 MV/3 mA output.[2] Reginato and Smith constructed a 600 kV/10 mA CW power supply with 18-stage driven by a 100 kHz oscillator.[3] Hara constructed a 3-stage 200 kV/200 mA output symmetrical Cockcroft-Walton (SCW) circuit using a 1 kHz power source.[4] Suematsu built a 3 MeV/6 mA electron accelerator of five stages driven by a 10 kHz converter.[5] In 1975, Reinhold reported a series of MV class and high output SCW generator working at 2 kHz.[6] Mizusawa of NHV Corporation developed the balance CW circuit generators in 3–3.6 kHz.[7] Su adopted 2.5 kHz as the operating frequency in the 600 kV/15 mA SCW power supply.[8]

However, these cascade generators driven by mid-range frequency power supply or generator are of reduced power efficiency. In some special case, such as electron beam flue gas treatment, it needs the power efficiency to be as high as possible. To increase the power efficiency, we think it necessary to employ the available line power source directly, and a 1.2 MV/50 mA power source of 3-stage SCW circuit was developed, using sulfur hexafluoride (SF_6) at 6.5 atm for insulation. It is of simple structure, low cost, easy maintenance, and high efficiency. A block diagram of the power supply is shown in Fig. 1.

II. CIRCUIT DESIGN

The CW-type of voltage multiplier circuit has been studied extensively, and formulas describing characteristics of the circuit are available in literatures.[5,6,8–13] They are suitable for calculating 50-Hz driven circuit after considering certain factors.

A. Voltage drop

With an input voltage of $V_a \sin\omega t$ to an N stages circuit, the output voltage will be given by

$$V = (2NV_a - \Delta V)\,F, \tag{1}$$

where $2NV_a$ is the theoretical non-load voltage, ΔV is the total load-dependent voltage drop, and F is the voltage efficiency related with capacitive voltage drop.

The total load-dependent voltage drop is contributed by V_C, V_R, and V_{Ls}, which are voltage drops caused, respectively, by the charge and discharge of the capacitors, the forward resistance of the rectifiers, and the leak inductance of the step-up transformer. It can be expressed as

$$\Delta V = \left(\Delta V_C^m + \Delta V_R^m + \Delta V_{Ls}^m\right)^{1/m}, \tag{2}$$

where $m = 3$, according to the experience of intermediate frequency power.[8] At $f = 50$ Hz condition, the voltage drops can be calculated by Eqs. (3)–(5),

$$\Delta V_C = \frac{I}{2f}\sum_{n=1}^{N}\left[\frac{n^2}{C_n} + \frac{1}{2C_{s(n)}}(1-\varepsilon)\right], \tag{3}$$

$$\Delta V_R = (3\pi)^{2/3} N V_a \left(\frac{R_t + R_D}{V_0}\frac{I}{2}\right)^{2/3}, \tag{4}$$

$$\Delta V_{L_s} = 2.32 N V_a \left(\frac{\omega L_s}{V_a}\frac{NI}{2}\right)^{1/2}, \tag{5}$$

where I is the load current; C_n and $C_{s(n)}$ are, respectively, the capacitance value of each stage in the coupling column and smoothing column; ϵ is the duty ratio, i.e., the charging duration over one cycle of the capacitor in the smoothing column (we note that the charging lasts quite a long time, unlike

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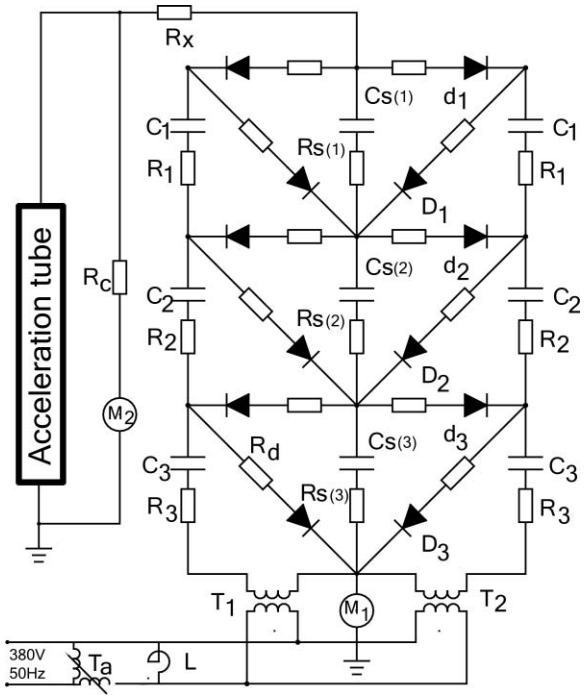

FIG. 1. Block diagram of 1.2 MV/50 mA symmetrical Cockcroft-Walton generator driven by 50 Hz. C_1, C_2, and C_3: coupling capacitor; Cs: smoothing capacitor, $C_{s(1)} = C_{s(2)} = C_{s(3)} = C_s$; d_1, d_2 and d_3; D_1, D_2 and D_3: rectifier; R_1, R_2 and R_3; $R_{s(1)}$, $R_{s(2)}$ and $R_{s(3)}$: current-limiting resistor; R_d: current-limiting resistor of rectifier; R_c: measuring resistor; R_x: damping resistor; T_a: regulating transformer; L: inductor; T_1 and T_2: step-up transformer; M_1: amperemeter for load current measurement; M_2: amperemeter for output voltage measurement.

the intermediate frequency case); R_t and L_s are the resistance and the leak inductance of the step-up transformer; R_D is the forward resistance of the rectifier, including the series resistance R_d, and $\omega = 1/f$.

For an N-stage circuit, the voltage efficiency is related to the ratio B of the capacitance of each stage to the equivalent capacitance of each rectifier considering the stray capacitance, given by Eq. (6),[4]

$$F = \frac{\sqrt{B/2}}{N} \tanh\left(\frac{N}{\sqrt{B/2}}\right). \tag{6}$$

In the 50 Hz driven SCW circuit, the B value is about 10^4. Then, while the stage number is limited to a handful number, so the F value approaches 1. This means the capacitive voltage drop can be neglected. However, as shown in Fig. 2, the voltage drops in the capacitors, rectifiers, and secondary winding are very large due to the high power output (the data marked with ○ were simulated by PSpice). This is a major factor in the power supply design.

B. Voltage ripple

When output voltage of the multiplier circuit is small, the waveform of voltage can be predicted by theoretical calculation.[14] The voltage ripple has two components: the capacitive part and load-dependent part. For an SCW circuit, the capacitive ripple δV_c is given by

$$\delta V_c = \frac{|V_L - V_R|\, B^{-1/2} \sinh^2(NB^{-1/2})}{\cosh(2NB^{-1/2}) \sinh(B^{-1/2})}, \tag{7}$$

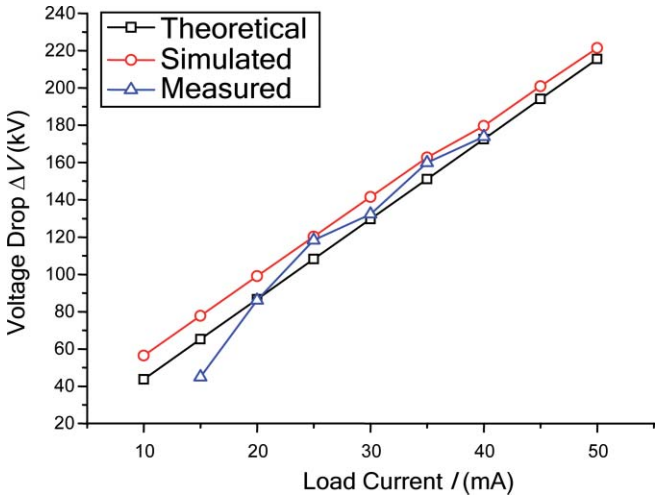

FIG. 2. (Color online) Voltage drop vs load current of the SCW generator.

where V_L and V_R are the peak value of the driving voltage of the left and right step-up transformer.[15] The δV_c equals to zero when the two transformers are of symmetrical uniformity.[4] This component of voltage ripple is essential in ultra-high voltage electronic microscope, but can be neglected in the high load current output. This is especially true in our case, where the voltage ripple is determined by

$$\delta V = \frac{I}{2f} \sum_{n=1}^{N} \frac{1}{C_{s(n)}} (1 - \varepsilon), \tag{8}$$

which means that the major component is dependent on load, as shown in Fig. 3.

Figure 4 shows the voltage and load current waveforms at 1.2 MV/50 mA output. The waveforms are complex when the output voltage is much high. The upper curve is high-voltage output, while the lower curve is the load current, both are ac waveform. The measured dc current at high-voltage is 83.5 μA, while the load current is 50 mA. The sampling resistor in the probe is 19.16 kΩ for voltage ripple and 2.17 Ω for load current ripple.

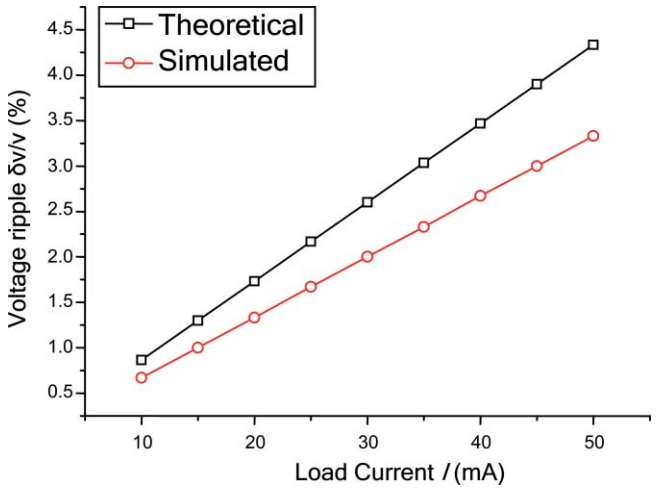

FIG. 3. (Color online) Voltage ripple vs load current current of SCW generator.

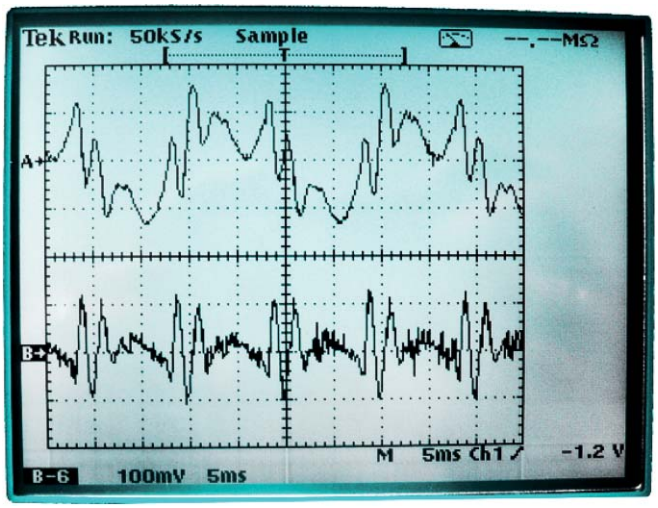

FIG. 4. (color online) High voltage and load current waveforms of the SCW generator at 1.2 MV/50 mA output.

The measured peak-to-peak (p-p) amplitude of the high voltage ripple is 300 mV, with the root-mean-square (RMS) value of 74.09 mV, and the p-p value of load current is 232 mV, with the RMS value of 40.09 mV. The ratio of high voltage ripple to high voltage output is 9.4% calculated using the half of p-p value. Although this is over two times larger than the theoretical ratio (4.4%), it is less than half of the theoretical voltage ripple in a traditional CW circuit, and is below the limit of the industrial application.

The large difference between the measurement and calculation results may be due to asymmetry of the circuit. The calculation is based on an ideal symmetrical circuit, but a real circuit may possess many asymmetrical factors, such as the diode conduction and the step-up transformers. Finer research has been done around the harmonics of the ripple, that the circuit asymmetry cause odd harmonics, while the asymmetry in charge-discharge process of capacitors cause the even harmonics.[16] The odd harmonics of the ripple increase with the load current. The asymmetry in charging and discharging current affects the load current measurement in that it causes two peaks in the curve, but this can be eliminated by adopting a parallel capacitor in the measurement circuit.

C. Choice of the parameter *N*

It can be seen from Eqs. (3)–(5) and (8) that by increasing the driving frequency or capacitance of each stage, the voltage drop and ripple can be limited in a reasonable range at increased load current or a large number of stages *N*. For fixed values of f, V_a, and I, an optimum N can be found for desired high-voltage output and the ripple. When $C_n = C_{s(n)} = C$, the relations of voltage output and ripple to N is shown in Figs. 5 and 6. In our power supply, we chose $N = 3$ in the circuit design, with $C_s = 18.75$ nF, $C_1 = C_2 = 28.13$ nF, and $C_3 = 45$ nF.

III. ANALYSIS OF THE RECTIFIER'S WORKING STATUS AND CONDUCTION ANGLE

A rectifier does not work in a continual status while the circuit is working. It allows the current to pass only in its operating time section in one cycle. Therefore, it is necessary to calculate conduction angle of the circuit to obtain the operation current and determine overall characteristics of the power supply. The numbers for the rectifiers, capacitors, and their voltages are given in Table I. The subscript s denotes the capacitors in the smoothing column; L and R represent the left and right side capacitors in the coupling column. The number of stage is 1–*N* from the high voltage terminal to the low end. The rectifiers are symmetrical, and are of two classed of d and D in one stage (Table II).

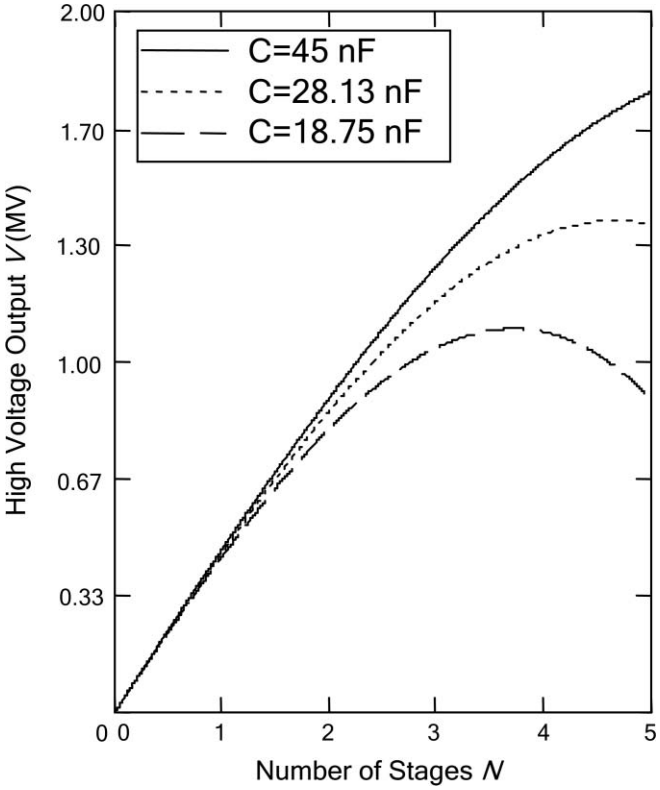

FIG. 5. Output voltage of SCW generator having different number of stages.

For the potentials of left and right input of $U_L(t) = V_a\cos(\omega t)$ and $U_R(t) = -V_a\cos(\omega t)$, the initial potential of the left side is V_a, and $-V_a$ of the right side. The phase

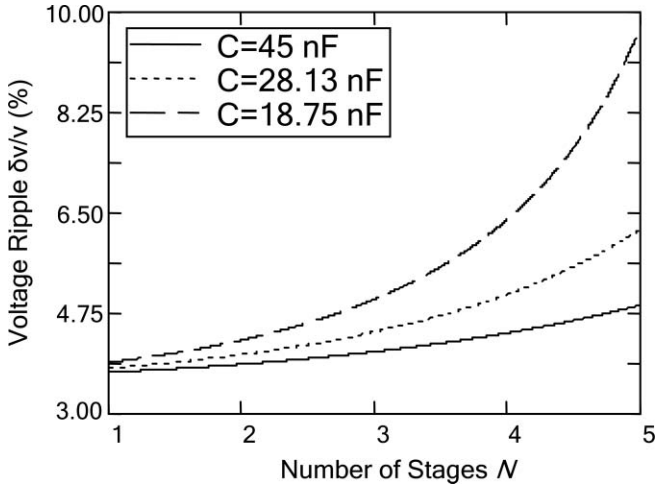

FIG. 6. Voltage ripple of SCW generator having different number of stages.

TABLE I. Numbers for the *N*-stages circuit.

Number	C_L	C_s	C_R
1	$V_{L(1)}$	$V_{s(1)}$	$V_{R(1)}$
...	...	...	...
n	$V_{L(n)}$	$V_{s(n)}$	$V_{R(n)}$
...	...	...	...
$N-1$	$V_{L(N-1)}$	$V_{s(N-1)}$	$V_{R(N-1)}$
N	$V_{L(N)}$	$V_{s(N)}$	$V_{R(N)}$

diagram of input potential U_L and the a, b, c, and d status are shown in Fig. 7. At point a, voltages of the smoothing capacitors reach the highest, voltages of the left coupling capacitors reach the highest, but voltages of the right coupling capacitors reach the lowest as they charge to the smoothing capacitors. At point c, voltages of smoothing capacitors also reach the highest, but the voltage status of left and right column capacitors are opposite to point a. Points b and d are lowest voltage output status. The charging circulations of d→a and b→c are shown, respectively, in Figs. 8(a) and 8(c), and the load discharging a→b or c→d are shown in Fig. 8(b).

The output charge of the load in each periodicity is

$$\Delta Q = IT, \tag{9}$$

where I is load current and T is the periodicity. For the N-stage generator, voltage of each capacitor in each stage can be calculated as follows:

Voltages of capacitors in the smoothing column are

$$\begin{cases} V_{s(1)} = 2V_a - \dfrac{\Delta Q}{2}\displaystyle\sum_{i=1}^{N}\frac{i}{C_i} \\ \cdots \\ V_{s(n)} = 2V_a - \dfrac{\Delta Q}{2}\displaystyle\sum_{i=n}^{N}\frac{i}{C_i} \\ \cdots \\ V_{s(N-1)} = 2V_a - \dfrac{\Delta Q}{2}\displaystyle\sum_{i=N-1}^{N}\frac{i}{C_i} \\ V_{s(N)} = 2V_a - \dfrac{\Delta Q}{2}\displaystyle\sum_{i=N}^{N}\frac{i}{C_i} \end{cases}. \tag{10}$$

Voltages of capacitors in the coupling column of the right side are

$$V_{R(n)} = \begin{cases} V_{s(n)}, & n = 1, 2, ..., N-1 \\ V_{s(N)} - V_a, & n = N \end{cases}. \tag{11}$$

Voltages of capacitors in the coupling column of the left side are

$$V_{L(n)} = \begin{cases} V_{s(n+1)}, & n = 1, 2, ..., N-1 \\ V_a, & n = N \end{cases}. \tag{12}$$

To simplify the calculation, we take an approximation that status a or c corresponds to the wave crest or the wave hollow of $U_L(t)$. After point a or c, both coupling columns keep the voltage, while the smoothing column discharging through load current, then output voltage comes to point b or d. The smoothing capacitors get the minimum voltage at the two points. The procession b→c is that the coupling capacitors of the left side begin to discharge to the smoothing capacitors, while the smoothing capacitors discharge to the coupling capacitors of the right side, see Fig. 8(c). However, during procession d→a, it is opposite that the coupling capacitors of left side begin to be charged from the smoothing capacitors, while the smoothing capacitors are charged from the coupling capacitors of the right side, see Fig. 8(a). As the circuit's symmetry, it is only needed to consider procession a→b to find the conduction time of rectifiers. In the load discharging process a→b, voltages of the smoothing capacitors are

$$V_{s(n)}(t) = V_{s(n)} - \frac{It}{C_s}, \quad n = 1, 2, ..., N. \tag{13}$$

For class d rectifiers in the left side, the backward voltages are given by

$$V_{d(n)}(t) = V_a(1 + \cos\omega t) - \frac{\Delta Q}{2}\sum_{i=n}^{N}\frac{i}{C_i} - (N - n + 1)\frac{It}{C_s}, \quad n = 1, 2, ..., N. \tag{14}$$

For class D rectifiers in the right side, the backward voltages are given by

$$V_{D(n)}(t) = V_a(1 + \cos\omega t) - \frac{\Delta Q}{2}\sum_{i=n}^{N}\frac{i}{C_i} + (N - n)\frac{It}{C_s}, \quad n = 1, 2, ..., N. \tag{15}$$

The duty time of the d and D class rectifiers, i.e., $t_{d(n)}$ and $t_{D(n)}$ can be solved by defining

$$V_{d(n)}(t) = 0, \quad V_{D(n)}(t) = 0, \quad n = 1, 2, ..., N. \tag{16}$$

The operation section time $T_{d(n)}$ and $T_{D(n)}$ can be obtained by

$$T_{d(n)} = T/2 - t_{d(n)}, \quad T_{D(n)} = T/2 - t_{D(n)}, \quad n = 1, 2, ..., N. \tag{17}$$

Some useful inferences can be derived from the solutions: the duty ratios are

$$\varepsilon_{d(n)} = 2T_{d(n)}/T, \quad \varepsilon_{D(n)} = 2T_{D(n)}/T, \quad n = 1, 2, ..., N; \tag{18}$$

the mean currents in the operation section time are

$$I_{d(n)} = \Delta Q/(2T_{d(n)}), \quad I_{D(n)} = \Delta Q/(2T_{D(n)}), \quad n = 1, 2, ..., N; \tag{19}$$

TABLE II. Symbols of the rectifiers and their backward voltages.

Number	d_1	D_1	...	d_n	D_n	...	d_{N-1}	D_{N-1}	d_N	D_N
Backward voltage	$V_{d(1)}$	$V_{D(1)}$	...	$V_{d(n)}$	$V_{D(n)}$	...	$V_{d(N-1)}$	$V_{D(N-1)}$	$V_{d(N)}$	$V_{D(N)}$

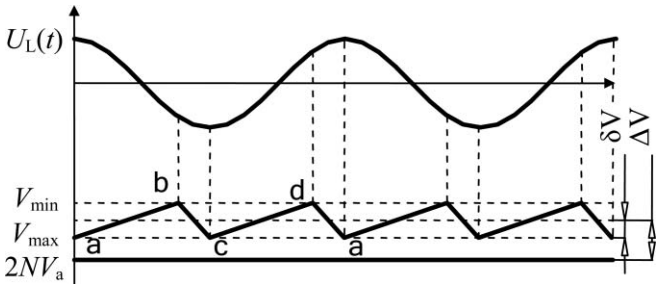

FIG. 7. Phase diagram of U_L and output voltage of the SCW generator.

and the peak currents passing the secondary winding are

$$I_d = \beta \sum_{n=1}^{N} \frac{\Delta Q}{2T_{d(n)}}, \quad I_D = \beta \sum_{n=1}^{N} \frac{\Delta Q}{2T_{D(n)}}, \tag{20}$$

where β can be 1.35 for an averaged benefit of the parameters. In Table III, the calculated and simulated duty time and duty ratio of the rectifiers are compared.

From Table III, one sees that the class d rectifier is conducted earlier than the class D rectifier in the same stage, because $V_{d(n)} - V_{D(n)} = -(2N - 2n + 1)It/C_s$. The deviations between the theoretical and simulated results could be due to two factors: the mean current approximation and the neglected voltage loss caused by the upper stage connection current.

IV. POWER FACTOR AND ITS COMPENSATION CONSIDERING THE EQUIVALENT CAPACITANCE

A. Power factor (*PF*) of the SCW circuit

A voltage multiplier power source is an ac to dc rectification power supply. The energy load is provided uninterruptedly by capacitors that are charged interruptedly by the ac power. Although the input voltage is sinusoid, the input current may be in a waveform of serious distortion. The *PF* is expressed as

$$PF = \frac{I_1}{\sqrt{\sum_{k=0}^{\infty} I_k^2}} \cos\varphi = \gamma\lambda, \tag{21}$$

TABLE III. Comparison of theory and simulation about rectifiers' connection.

Rectifiers		d_1	D_1	d_2	D_2	d_3	D_3
Duty time t (ms)	Theoretical	6.46	8.08	6.94	7.99	7.85	8.33
	Simulated	6.20	7.40	7.50	7.80	8.20	8.50
Duty ratio ϵ	Theoretical	0.354	0.192	0.306	0.201	0.215	0.167
	Simulated	0.380	0.260	0.250	0.220	0.180	0.150

where I_1 and I_k are the RMS values of the current components, φ is the phase difference between the voltage and the fundamental component of the current, γ is called distortion factor, and λ is called displacement factor. The input voltage and current waveforms simulated by the PSpice are as shown in Fig. 9. The phases of voltage and current are not synchronized, hence a need of *PF* compensation by displacement factor correction.

B. Power factor correction for the SCW circuit

The existence of parasitic capacity would become a capacitive load, especially for capacitors of rectifiers and filters. The capacitive load creates reactive power, and a big enough reactive current would affect the stability of the step-up transformers and the power system.

The equivalent capacitance of the power circuit can be analyzed.[17] For an *N*-stage SCW circuit, the charging currents are show in Figs. 8(a) and 8(c), both the charging currents are the same but charging and discharging roles are alternated for the right and left coupling column in the procession b→c and the procession d→a. In Fig. 8(a), $i_{D(1)}$, ..., $i_{D(n)}$, ..., $i_{D(N-1)}$, and $i_{D(N)}$ are the charging currents from the smoothing column to the left coupling column. They can be considered as *N*-branch parallels. The capacitances of each branch are

$$\frac{1}{C_{D(n)}} = \sum_{i=n}^{N} \frac{1}{C_i} + \frac{N-n}{C_s}, \quad n = 1, 2, ..., N. \tag{22}$$

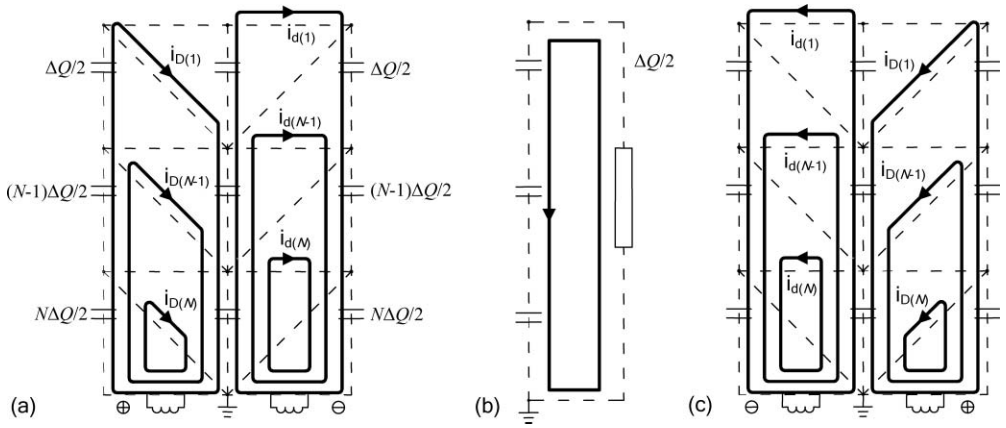

FIG. 8. (a) Charge circulation during d→a. (b) Load discharging. (c) Charge circulation during b→c.

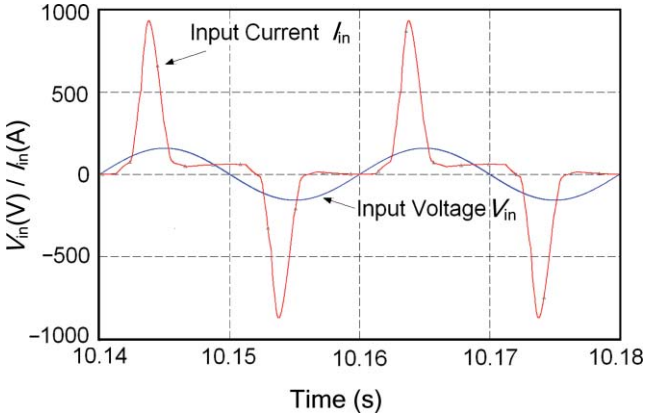

FIG. 9. (Color online) Input voltage and current waveforms.

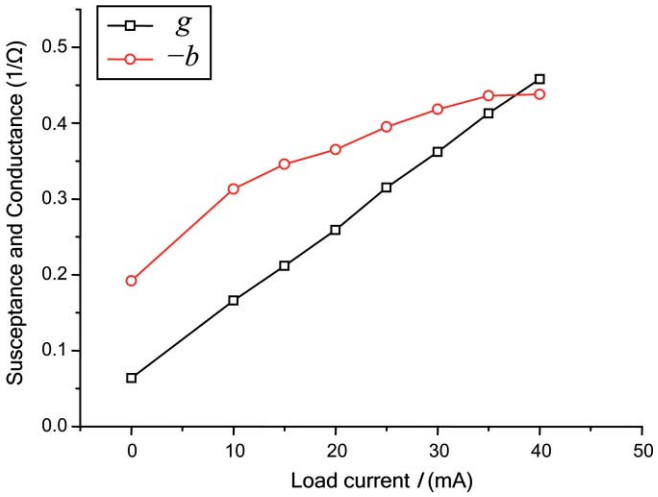

FIG. 10. (Color online) Conductance and susceptance vs load current.

Taking an approximation that they are conducted at the same time, the equivalent capacitance is

$$C_{\mathrm{D}} = \sum_{i=1}^{N} C_{\mathrm{D}(i)}. \tag{23}$$

While $i_{\mathrm{d}(1)}$, …, $i_{\mathrm{d}(n)}$, …, $i_{\mathrm{d}(N-1)}$, and $i_{\mathrm{d}(N)}$ are the charging currents from the right coupling column to the smoothing column, $C_{\mathrm{d}(n)}$ and C_{d} can be considered similarly,

$$\frac{1}{C_{\mathrm{d}(n)}} = \sum_{i=n}^{N} \frac{1}{C_i} + \frac{N-n+1}{\mathrm{C_s}}, \quad n = 1, 2, ..., N, \tag{24}$$

$$C_{\mathrm{d}} = \sum_{n=1}^{N} C_{\mathrm{d}(n)}, \tag{25}$$

where $C_{\mathrm{d}(n)}$ are the capacitances of each branch and C_{d} is the total capacitance. Then the equivalent capacitance C_{e} is

$$\frac{1}{C_{\mathrm{e}}} = \frac{1}{C_{\mathrm{D}}} + \frac{1}{C_{\mathrm{d}}}. \tag{26}$$

Considering the characteristic of the rectifiers, the equivalent capacitance is effective only in the duty section time, so the capacitive impedance X_{e} of the whole circuit can be

$$X_{\mathrm{e}} = \frac{1}{\omega}\left(\frac{1}{\sum_{n=1}^{N} \varepsilon_{\mathrm{d}(n)} C_{\mathrm{d}(n)}} + \frac{1}{\sum_{n=1}^{N} \varepsilon_{\mathrm{D}(n)} C_{D(n)}}\right). \tag{27}$$

For the 3-stage circuit at 50 mA load current, $X_{\mathrm{e}} = 8.311 \times 10^5\ \Omega$. This means the compensation inductance can be 10 mH.

The measurements of the conductance g and susceptance b are shown in Fig. 10, which shows increased linearity of the equivalent conductance. The experimental results indicate that the susceptance is of capacitive characteristics. By extrapolation of the experimental result, it gets that g is 0.559 Ω^{-1} and b is -0.448 Ω^{-1} in the 1.2 MV/50 mA output condition. In this case, the equivalence value of power factor is $\cos(\mathrm{arctg}(b/g)) = 0.78$, the power efficiency is 0.839 with 371 V/247 A input. To balance the capacitive susceptance $-0.448\ \Omega^{-1}$ at 50 mA output, it needs a compensation inductance of 7.11 mH. The compensation difference is due to leak inductance of transformer.

V. PROTECTION RESISTANCE OF THE CIRCUIT

A good design of SCW power supply needs a suitable resistance to protect it, in case of short circuit, from serious damage to the electrical elements of the power supply. Researches have indicated that the highest and lowest rectifier are the most likely to be subjected to this kind of damage, but other rectifiers are far less to be damaged.[18,19] For a silicon rectifier, the junction should be protected against excessive heating effect, so the overflow ability can be a certain value I_{m} which usually calculated as

$$\int_0^{T_{\mathrm{m}}/2} (I_{\mathrm{m}} \sin \omega t)^2 dt = \frac{1}{4} T_{\mathrm{m}} I_{\mathrm{m}}^2, \tag{28}$$

where T_{m} is the periodicity of I_{m}. In a short circuit incident, the surge current $i(t)$ is non-sine, but its heat effect in the rectifier is in direct ration of $\int_{0\to\tau} i^2(t)\mathrm{d}t$, where τ is the short circuit section time. If $\int_{0\to\tau} i^2(t)\mathrm{d}t$ is smaller than $T_{\mathrm{m}}{I_{\mathrm{m}}}^2/4$, the electronic component cannot be damaged.

In developing the 50-Hz SCW power supply, we found that the class d rectifier in the first stage would be damaged, and also would the class d rectifier in the second stage. In both situations, the class D rectifier in end stage was damaged. As the duration in the short-circuit transition is shorter than the operation periodicity, inductive reactance of secondary branch of the transformer is much larger than the resistance of the rectifier branch. So it can be considered that the surge passed through the class D rectifier in the end stage, from the ground potential to the high-voltage output, then short circuit to the ground, it is equivalent to a simple RC discharge circuit as $u - iR = 0$, $i = -cdu/dt$, that is,

$$\frac{du}{dt} + \frac{1}{Rc} u = 0. \tag{29}$$

The solution of Eq. (29) is $u(t) = u_0 \exp(-t/Rc)$, or $i(t) = (u_0/R)\exp(-t/Rc)$. In the SCW circuit, c is the total

capacitance of one side coupling column except the capacitor in *N*th stage, R is the total resistance in the short-circuited loop, and u_0 is the total voltage of the capacitors in the short-circuited loop. The c, R, and u_0 are given by

$$c = \left[\sum_{n=1}^{N-1} \frac{1}{C_n}\right]^{-1}, \tag{30}$$

$$R = R_{\mathrm{x}} + \sum_{n=1}^{N-1} R_n, \tag{31}$$

$$u_0 = \sum_{i=1}^{N-1} V_{\mathrm{s}(n)}. \tag{32}$$

Assuming that the duration in the short-circuit transition is τ, the heat effect of surge current in the rectifier D_N can be given by

$$\int_0^{\tau} i^2(t)dt = \frac{u_0^2 c}{2R}[1 - e^{-2\tau/Rc}]. \tag{33}$$

The critical value is $T_{\mathrm{m}}{I_{\mathrm{m}}}^2/4$, so the safety resistance R_0 of R shall satisfy Eq. (34),

$$\frac{2u_0^2 c}{I_{\mathrm{m}}^2 R_0 T_{\mathrm{m}}}[1 - e^{-2\tau/R_0 c}] = 1. \tag{34}$$

The τ value is in the range of 10—1000 μs, and this is much smaller than $R_0 c$. Using the first approximation, solution of Eq. (34) can be

$$R_0 = 2\frac{u_0}{I_{\mathrm{m}}}\sqrt{\frac{\tau}{T_{\mathrm{m}}}}. \tag{35}$$

From Eq. (35), the safety resistance R_0 is related to the capacitor voltage and the duration τ, when the rectifiers with certain overflow ability are selected. For higher safety coefficient, it is necessary to select the maximum working current as the I_{m} value. In our experiment, Eq. (35) satisfies the circuit design.

VI. CONCLUSION

Design specifications of the power supply have been achieved, with up to 1.32 MV of its non-load voltage, and the power efficiency of over 83% at 1.2 MV/50 mA output. This prototype power supply indicates that SCW circuit can be driven by line-frequency power directly. This is of help in improving the efficiency of power supply, an important factor for industrial electron beam irradiator.

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